Claims Amendments

Please replace the previous claims with the claims listed below.

Claims 1-67 (canceled)

68. (new) A method of digital signal processing of multi-sampled phase (DSP MSP), recovering data from a received signal [cl.65], which comprises capturing multiple samples of the signal per a symbol time [cl.29] with a sampling clock or its sub-clocks defining known phase displacements versus the sampling clock [cl.29]; the DSP MSP method [&2/p.8] comprising the steps of:

detection of phases of rising and falling edges of the signal [cl.66] by using said signal samples captured at said known phase displacements [cl.29];

evaluation of a length of a pulse of the signal by using said phases of signal edges [cl.66];

calculation of a number of data bits received in the pulse by using said evaluation of the pulse length [cl.66].

69. (new) A method as claimed in claim 68, comprising use of multiple sequential processing stages or parallel processing phases of said captured samples; wherein:

said sequential processing stages are driven by the sampling clock or clocks synchronous to the sampling clock [&3/p.2, cl.1, cl.2];

consecutive said parallel processing phases are driven by clocks which are shifted in time by corresponding consecutive periods of said sampling clock and have 2 or more times lower frequencies [&3-5/p.3, cl.11], in order to multiply processing times assigned for said parallel phases [&3-5/p.3, cl.11];

outputs of a one parallel processing phase are passed to a next parallel phase [&4-5/p.4, cl.18], wherein output register bits of the original parallel phase are re-timed by clocking them into an output register of the next parallel phase simultaneously with processing results of the next parallel phase [&4-5/p.4, cl.18, cl.19];

said passed outputs are used by a following sequential processing stage which belongs to the next parallel processing phase [cl.18, cl.19].

70. (new) A method of digital signal processing of multi-sampled phase (DSP MSP), recovering data from a received signal [cl.65], which comprises capturing multiple samples of the signal per a symbol time [cl.29] with a sampling clock or its sub-clocks defining known phase displacements versus the sampling clock [cl.29]; the DSP MSP method [&2/p.8] comprising the steps of:

filtering out noise from said captured signal with digital filters [cl.67, &1-4/p.6];

detecting phases of rising and falling edges of the resulting filtered signal [cl.66] derived from said signal samples captured at said known phase displacements [cl.29];

evaluation of a length of a pulse of the filtered signal by using said phases of filtered signal edges [cl. 66];

calculation of a number of data bits received in the pulse by using said evaluation of the pulse length [cl.66].

71. (new) A method as claimed in claim 70, wherein said evaluation of pulse length comprises the steps of:

defining an edge skew, between an edge of the sampling clock and the signal edge, with the time displacement of sub-clock which captures a change in a signal level [cl.49];

measuring said pulse length as being composed of such edge skew of a front edge of the incoming waveform, an integer number of sampling clock periods between the front edge and an end edge, and such edge skew of the end edge of the waveform [cl.49].

72. (new) A method of digital signal processing of multi-sampled phase (DSP MSP) for recovering data from a received signal waveform, captured with a sampling clock or its sub-clocks [&2/p.8], by processing length of inter-transition intervals of the captured waveform [&7-9/p.11, &6-8/p.12]; the DSP MSP method comprising the steps of:

capturing multiple samples of said received signal during every symbol time by the sampling clock or its sub-clocks [&2/p8, cl.29];

detecting transition times of the received signal waveform by processing said captured samples [&7-9/p.11, FIG.3A, cl.49];

measuring said length of inter-transition interval occurring between said transition times [&1-2/p.3, &6-8/p.12, cl.66];

calculating a number of data bits received during the inter-transition interval by evaluating said lengths

of inter-transition interval [&2/p.8, &6-8/p.12, cl.66].

73. (new) A method of synchronous sequential processing (SSP) for sampling and capturing and processing of a waveform [cl.1, cl.4, cl.5], wherein said waveform sampling and capturing use a sampling clock or outputs of a sampling clock delay line [cl.4, cl.5] and said waveform processing uses multiple sequential processing stages [cl.1] or multiple parallel processing phases [cl.11]; wherein the SSP method comprises the steps of:

driving said sequential processing stages with clocks synchronous to said sampling clock,

and performing a cumulative processing operation split into a series of consecutive basic operations implementing addition or subtraction or comparison [spec.&4/p.5 and spec.&10/p.13 - &2/p.14 and FIG.3A] wherein a result of one basic operation performed earlier [such earlier operation result representing a front edge skew is preserved in 1FER until an end edge is detected after all the basic operations occurring in between, as shown in spec.&10/p.13 - &2/p.14 and FIG.3A] is used for processing [such processing shown in &1-2/p.14 and FIG.3A, calculates the phase skew between the front edge of the data string and the end edge] a result of another basic operation performed later [such later result representing an end edge skew is provided by 1EER when an end edge is detected after all the basic operations occurring in between, as shown in spec.&10/p.13 - &2/p.14 and FIG.3A];

or driving said parallel phases with clocks synchronous to said sampling clock wherein consecutive parallel phases are driven by clocks shifted in time by one or more periods of the sampling clock [cl.11],

and passing outputs of a one parallel phase to a next parallel phase in order to use said passed outputs for processing conducted by a following stage of the next parallel phase [spec. &4-5/p.4, cl.18] wherein said outputs passing is performed by re-timing output register bits of the one phase by clocking them into an output register of the next parallel phase simultaneously with processing results of the next parallel phase [spec. &4-5/p.4, cl.19];

wherein said use of earlier sequential operation result for processing later sequential operation result or said passing of outputs of one parallel phase to next parallel phase, enables continuous processing of indefinite waveform interval carrying high frequency pulses.

74. (new) An SSP method as claimed in claim 73 comprising merging of said parallel processing

phases [cl.14], the SSP method comprising the step of:

merging said multiple parallel processing phases into a smaller number of parallel phases or into a single processing phase, when passing from a one sequential processing stage to a next sequential stage[cl.14];

wherein clocking frequency of such merged phase equals to a sum of clocking frequencies of said parallel phases which are clocked into the merged phase [see &7/p.11 and FIG.3A showing merging of phase 11DFR clocked by 11Clk1 with phase 12DFR clocked by 12Clk1 into phase 1DFR clocked by 1Clk2, wherein 1Clk2_frequency =11Clk1_frequency +12Clk1_frequency].

75. (new) An SSP method as claimed in claim 73, comprising utilization of said synchronous sequential stages or said parallel processing phases for noise filtering from the processed waveform, the SSP method comprising the steps of:

clocking-in a carry over part of an output register of a first filter stage of said one parallel phase into an output register of the first filter stage of the next phase together with filtering results of the next phase [&4/p.6, cl.47];

using said clocked in part of output register of first filter stage of one phase by a second filter stage of said next phase for filtering noise from a wave-form interval which extends through both said parallel phases [&4-5/p.4, &4/p.6, cl.47].

76. (new) An SSP method as claimed in claim 73, wherein:

said sequential processing stages use selectors or arithmometers or output registers [cl.23].

77. (new) An SSP method as claimed in claim 76 wherein said waveform processing further comprises use of multiple parallel processing stages; wherein;

said multiple parallel processing stages, performing different logical or arithmetical operations, are driven by the same clock which is applied simultaneously to all the parallel stages [cl.20].

78. (new) An SSP method as claimed in claim 73 further comprising use of a programmable control unit (PCU)) for implementing programmable or adaptive signal processing algorithms [&2-3/p.2]; the SSP method comprising the steps of:

using said waveform processing, utilizing said sequential processing stages or said parallel processing

phases, for real time capturing and processing of an in-coming waveform [spec.&2-3/p.2, cl.1];

using said PCU for reading results of the waveform processing from said synchronous sequential stages or said parallel processing stages and for controlling operations of the waveform processing [&2-3/p.2, &1-2/p.6, &3-4/p.7, &1-4/p.28, cl.61-64].

79. (new) An SSP method as claimed in claim 78, the SSP method further comprising:

screening and capturing of the incoming signal with a wave-form screening and capturing circuits (WFSC) controlled by the PCU [spec.&1-4/p.28, cl.57-60, cl. 64].

80. (new) An SSP method as claimed in claim 79, wherein the SSP method further comprises:

using said WFSC for verification of said captured waveforms for compliance or non-compliance with programmable patterns [cl.57] and for buffering captured waveform for which the preprogrammed compliance or said non-compliance has been detected [cl.59];

wherein said programmable patterns are provided by the PCU and such buffered waveform is read by the PCU [spec.&2-4/p.28]

81. (new) An SSP method as claimed in claim 79, wherein operations of said WFSC further comprise:

selecting a time interval for which incoming wave-form captures shall be buffered and communicated to the PCU [&2-4/p.28, cl.60-61];

wherein such slot selection is programmed by the PCU and such pre-selected buffered waveform is read by the PCU [spec.&2-4/p.28, cl.60-61].

82. (new) An SSP method as claimed in claim 73, comprising correction of cumulative error, in measuring length of incoming signal pulse, caused by periodical phase skews [&5-8/p.17, cl.51]; the SSP method comprising the steps of:

using said periodical phase skew as an estimate of a phase skew between the sampling clock period and an expected period of a clock which drives the incoming signal [cl.51];

calculating an accumulation of said periodical phase skews for said signal pulse [cl.51];

using said periodical skew accumulation to correct a length of a data string detected in the signal pulse[this statement is supported by the &5-6/p.6, and by &5-8/p.17 wherein the term "registered number of sampling clocks" is synonymous with the term "length of data string detected".

Furthermore this statement narrows 2nd statements in both cl.50 and cl.52 to cases related to PSA embodiment shown in spec.&4-7/p.16].

83. (new) An SSP method as claimed in claim 82; further comprising the steps of:
reading a next set of said periodical phase skews from the PCU or other circuits [spec.&4-9/p.18] and attaching them to a present set of said periodical phase skews [cl.52];
synchronous communication of said periodical skew accumulation to phase processing stages [spec.&5-6/p.6] which use such skew accumulation to modify said length of said data string detected [spec.&4-7/p.16 and &5/p.17].

84. (new) A method of fractional bit staffing (FBS) for improving accuracy of fixed point arithmetic [spec.&2/p.5] for a long cumulative operation comprising a series of basic addition or subtraction operations [spec.&2-5/p.5, &5-8/p.17] between components of a processed argument [such as symbol time periods of said inter-transition interval of the received signal, named as Pe in &5-8/p. 17] and terms of a processing argument [such as sampling clock periods of the inter-transition interval, named as Ps in &5-8/p.17]; the FBS method comprising the steps of:
expressing said processing argument as a series of terms, wherein each term may have a differently staffed last bit or several last bits expressing a fractional value of the term [&3-4/p.5 and &5-8/p.17 wherein differently staffed bits are included in the periodical phase skew (Ps-Pe)];
combining said staffed last bits with previous bits expressing more significant constant part of the term in order to provide said term [spec.&3-4/p.5];
a series of such terms is provided for a repeatedly performed arithmetic operation [&3-4/p.5, &5-8/p. 17, cl.34);
using every said term of processing argument for processing performed during corresponding said basic operation [spec.&3-5/p.5];
wherein the FBS enables reduction of a total error of such long cumulative operation to a single last bit resolution [spec.&3-5/p.5].

85. (new) A method of fractional bit staffing (FBS) for improving accuracy of fixed point arithmetic [spec.&2/p.5] for a long cumulative operation comprising a series of basic addition or subtraction operations [spec.&2-5/p.5, &5-8/p.17] between components of a processed argument [such as

symbol time periods of said inter-transition interval of the received signal, named as Pe in &5-8/p. 17] and terms of a processing argument [such as sampling clock periods of the inter-transition interval, named as Ps in &5-8/p.17]; the FBS method comprising the steps of:

expressing said processing argument as a series of consecutive terms,

wherein each said term has a more significant constant part combined with a last bit or last bits staffed with a fractional value which may be different for said consecutive terms [&3-4/p.5 and &5-8/p.17 wherein such differently staffed bits are represented by the periodical phase skew (Ps-Pe)];

performing said cumulative operation by using said series of terms wherein each said term comprises said constant part and said staffed bit or bits [spec.&3-4/p.5, &5-8/p.17];

wherein the FBS enables reduction of a total error of such long cumulative operation to a single last bit resolution [spec.&3-5/p.5].

86. (new) An FBS method as claimed in claim 85, comprising correction of cumulative errors in measuring a lengths of an incoming signal inter-transition interval with a local sampling clock having periodical phase skews versus symbol periods expected in the incoming signal [&5-8/p.17]; wherein:

a series of said periodical phase skews is derived as estimates of a phase skew between a sampling clock period versus the expected symbol period anticipated for consecutive symbols sampled during the inter-transition interval, wherein said phase skew estimates may differ for said consecutive symbols [&5-8/p.17, cl.51];

the series of periodical phase skews, used as said differently staffed last bits expressing said fractional values, are combined with said sampling clock period, used as the more significant constant part of the terms, in order to produce said terms [&5-8/p.17, cl.51].

87. (new) A clock selection system (CSS) for enabling sub-clocks, generated by the outputs of serially connected gates which a sampling clock is propagated through, during particular phases [cl.9] corresponding to cycles of the sampling clock [cl.7]; wherein:

clock selectors connected serially are used for enabling said sub-clocks [cl.9, cl.13];

falling edges of said sub-clocks are used for driving said clock selectors selecting parallel processing phases during which positive sub-clocks are enabled [cl.9, cl.13];

or rising edges of said sub-clocks are used for driving said clock selectors selecting parallel processing

phases during which negative sub-clocks are enabled [cl.9, cl.13].